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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LEE, CHRISTOPHER E	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 04/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,707	JARAMILLO ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4 and 6-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4 and 6-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt was acknowledged of the Amendment filed on 28th of February 2006. Claims 1 and 13-16 had been amended; claims 17-19 had been canceled; and no claim had been newly added since the RCE Non-Final Office Action was mailed on 19th of August 2005.

2. Receipt is acknowledged of the Response to Non-Compliant Amendment filed on 23rd of March 2006. No claim has been amended; no claim has been canceled; and no claim has been newly added since the Amendment was filed on 28th of February 2006. Currently, claims 1, 2, 4, 8-23 and 25 are pending in this Application.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1, 2, 4, 6-9, and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peters et al. [US 6,636,927 B1; hereinafter Peters] in view of Hopkins [US 5,761,464 A] and Applicants' Admitted Prior Art [hereinafter AAPA].

Referring to claim 1, Peters discloses a bridge apparatus (i.e., RAID Controller 206 in Fig. 2), comprising:

- a first bus (i.e., Secondary PCI bus 218 of Fig. 2) adapted to facilitate data transfer (See col. 7, lines 37-38);
- a second bus (i.e., Primary PCI bus 204 of Fig. 2) adapted to facilitate data transfer (See col. 5, lines 52-54);
- a bridge (i.e., PCI-to-PCI Bridge 216 in Fig. 2) coupling said first bus to said second bus (See col. 6, lines 10-14),
    - said bridge adapted to perform memory read, memory read line, and memory read multiple commands from said first bus to said second bus (See col. 10, lines 30-64).

Peters does not teach that the bridge is configured to allow a PCI Master accessing the first bus to dynamically decide a prefetch size of data based on a PCI cycle type.

Hopkins discloses a prefetching variable length data (See Abstract), wherein

- a first bus (i.e., System Bus 10 of Fig. 1);
- a second bus (i.e., PCI I/O Bus 20 of Fig. 1); and
- a bridge (i.e., Interface Unit 30 of Fig. 1) coupling the first bus to the second bus (See col. 3, lines 39-41), wherein
    - the bridge (i.e., said Interface Unit) is configured to allow a PCI Master accessing the first bus to dynamically decide a prefetch size of data based on a PCI cycle type (See col. 5, line 64 through col. 6, line 20 and col. 9, lines 42-52, wherein in

fact that the prefetch size could vary dynamically depending upon the device that is making the read request on PCI bus impliedly suggests that the bridge is configured to allow a PCI Master (i.e., PCI device 40 in Fig. 1) accessing the first bus (i.e., System Bus 10 of Fig. 1) to dynamically decide a prefetch size of data based on a PCI cycle type (i.e., upon a read request signal from a specific PCI device)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said prefetching variable length data, as disclosed by Hopkins, in said bridge (i.e., PCI-to-PCI Bridge), as disclosed by Peters, for the advantage of making said bridge apparatus more efficient use of the bandwidth of the slower second bus, as compared to conventional approach (See Hopkins, col. 3, lines 5-22).

Peters, as modified by Hopkins, does not expressly teach second bus having cache memory, wherein the bridge apparatus is adapted to perform the memory read multiple command with the cache memory.

AAPA discloses a conventional PCI to PCI bridge handling a memory read multiple command (Fig. 2), wherein

- a second bus (i.e., Primary PCI Bus 240 of Fig. 1) has cache memory (See page 9, lines 1-3; i.e., wherein in fact that memory read multiple cycles are used typically when a device is accessing Cache memory implies that a second bus has cache memory), and
- a bridge apparatus (i.e., PCI to PCI bridge 250 and Primary/Secondary PCI Busses 215, 240 in Fig. 2) is adapted to perform memory read multiple command with the cache memory (See page 13, line 16 through page 14, line 11).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said means for handling said memory read multiple command, as

disclosed by AAPA, to said bridge apparatus, as disclosed by Peters, as modified by Hopkins, for the advantage of offering much higher read performance for high end system (See AAPA, page 9, lines 11-13).

Referring to claim 2, Peters teaches

- the memory read multiple command prefetches more data than the memory read command (See col. 9, lines 32-40; i.e., memory read multiple command prefetches multiple memory cache lines from a memory. However, memory read command prefetches only less than a cache line from the memory).

Referring to claim 4, Peters teaches

- the memory read multiple command prefetches more data than the memory read line command (See col. 9, lines 34-40; i.e., memory read multiple command prefetches multiple memory cache lines from a memory. However, memory read line command prefetches only one complete cache line from the memory).

Referring to claim 6, Peters teaches

- second bus (i.e., Primary PCI bus 204 of Fig. 2) has RAM memory (i.e., Main Memory (RAM) 214 of Fig. 2),
    - wherein the bridge apparatus (i.e., RAID Controller 206 in Fig. 2) is adapted to perform memory read multiple command with the RAM memory (See col. 6, lines 31-47).

Referring to claim 7, AAPA teaches

- the bridge (i.e., Host Bridge 230 in Fig. 2) having a prefetch buffer (i.e., Prefetch Buffer 232 of Fig. 2), wherein
    - the prefetch buffer is adapted to be flushed after a memory read multiple command by the first bus (i.e., Primary PCI Bus 240 of Fig. 2; See page 14, lines 9-11).

Referring to claims 8 and 9, Peters teaches

- the memory read multiple command utilizes at least 64 Dwords (See col. 9, lines 56-67; i.e., memory read multiple command utilizes a read prefetch buffers 702 in segment of which the size is 256 bytes, viz., 64 double words in Fig. 7).

Referring to claim 11, Peters teaches

- the first bus (i.e., Secondary PCI bus 218 of Fig. 2) is a PCI bus.

Referring to claim 12, Peters teaches

- the second bus (i.e., Primary PCI bus 204 of Fig. 2) is a PCI bus.

Referring to claim 13, Peters teaches

- the first bus (i.e., Secondary PCI bus 218 of Fig. 2) is adapted to support a SCSI disk controller (i.e., SCSI Adapters 220, 222 in Fig. 2).

Referring to claim 14, Peters teaches

- the second bus (i.e., Primary PCI bus 204 of Fig. 2) is a PCI bus.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peters [US 6,636,927 B1] in view of Hopkins [US 5,761,464 A] and AAPA as applied to claims 1, 2, 4, 6-9, and 11-14 above, and further in view of Bennett [US 6,510,475 B1].

Referring to claim 10, Peters, as modified by Hopkins and AAPA, discloses all the limitations of the claim 10, except that does not expressly teach that a prefetch size of a memory read multiple command is at least four times as large as said size of a memory read or memory read line command.

Bennett discloses a data fetching control mechanism (See Abstract and Fig. 2), wherein

- a bridge (i.e., P64H 140 of Fig. 1) including a data fetching control mechanism (i.e., CONTROL MEC 146 of Fig. 2), which sets up a prefetch size (e.g., row #8 in Fig. 4, Soft DT Request Length: pre-fetch 8 cache lines) of a memory read multiple command (i.e., cache line size 64 bytes, PCI freq. 66 Mhz, REQ64#-deasserted, and memory read multiple command) is at least four times as large as said size (i.e., row #7 in Fig. 4, Soft DT Request Length: pre-fetch 2 cache lines) of a memory read command (i.e., cache line size 64 bytes, PCI freq. 66 Mhz, REQ64#-deasserted, and memory read command). Refer to col. 7, line 1 through col. 8, line 11.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said data fetching control mechanism, as disclosed by Bell, in said bridge, as disclosed by Peters, as modified by Hopkins and AAPA, for the advantage of providing an efficient data fetching control mechanism which fetches optimized data from a memory subsystem on one side of said bridge (i.e., host bridge such as PCI-PCI bridge) for PCI devices on the other side of said bridge in accordance with characteristics of a particular request, such as a command type, a data width, a clock frequency and a cache line size (See Bennett, col. 2, lines 6-12).

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Corrigan et al. [US 5,983,306 A ; hereinafter Corrigan] in view of Hopkins [US 5,761,464 A].

Referring to claim 15, Corrigan discloses a controller apparatus (i.e., Bridge Circuit in Fig. 1), comprising:

- a first bus (i.e., Secondary I/O Bus 3 of Fig. 2) adapted to facilitate data transfer (i.e., for data transferring between Secondary Bus Master 30 and PCI bus bridge 1 in Fig. 1);
- a second bus (i.e., Primary I/O Bus 4 of Fig. 2) adapted to facilitate data transfer (i.e., for data transferring between Primary Bus Slaves 40, 50, 60 and PCI bus bridge 1 in Fig. 1; See col. 5, lines 1-4); and
- a controller (i.e., PCI bus bridge 1 of Fig. 2) coupling the first bus to the second bus (See col. 4, line 67 through col. 5, line 1),
    - the controller adapted to perform memory read, memory read line, and memory read multiple commands (See col. 3, lines 31-57) from the first bus (i.e., Secondary I/O Bus as an initiator) to the second bus (i.e., Primary I/O Bus as a target; See col. 5, lines 12-14).

Corrigan does not teach that the controller is configured to allow a PCI Master accessing the first bus to dynamically decide a prefetch size of data based on a PCI cycle type.

Hopkins discloses a prefetching variable length data (See Abstract), wherein

- a first bus (i.e., System Bus 10 of Fig. 1);
- a second bus (i.e., PCI I/O Bus 20 of Fig. 1); and
- a controller (i.e., Interface Unit 30 of Fig. 1) coupling the first bus to the second bus (See col. 3, lines 39-41), wherein
    - the controller (i.e., said Interface Unit) is configured to allow a PCI Master accessing the first bus to dynamically decide a prefetch size of data based on a

PCI cycle type (See col. 5, line 64 through col. 6, line 20 and col. 9, lines 42-52, wherein in fact that the prefetch size could vary dynamically depending upon the device that is making the read request on PCI bus impliedly suggests that the controller is configured to allow a PCI Master (i.e., PCI device 40 in Fig. 1) accessing the first bus (i.e., System Bus 10 of Fig. 1) to dynamically decide a prefetch size of data based on a PCI cycle type (i.e., upon a read request signal from a specific PCI device)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said prefetching variable length data, as disclosed by Hopkins, in said controller (i.e., PCI bus bridge), as disclosed by Corrigan, for the advantage of making said controller apparatus more efficient use of the bandwidth of the slower second bus, as compared to conventional approach (See Hopkins, col. 3, lines 5-22).

8. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peters [US 6,636,927 B1] in view of Hopkins [US 5,761,464 A].

Referring to claim 16, Peters discloses a method of operating (See Abstract and Fig. 5) a bridge (i.e., PCI-to-PCI Bridge 216 in Fig. 2) coupled between a first bus (i.e., Secondary PCI bus 218 of Fig. 2) and a second bus (i.e., Primary PCI bus 204 of Fig. 2; See col. 6, lines 10-14), comprising:

- a PCI Master (i.e., PCI master device, e.g., RAID Processor 224 of Fig. 2) initiating a read multiple command on the first bus (i.e., said Secondary PCI bus; See col. 6, lines 30-43);

- the bridge (i.e., said PCI-to-PCI Bridge) passing the read multiple command to a target (i.e., selected PCI slave device, e.g., Main Memory (RAM) 214 of Fig. 2) on the second bus (i.e., said Primary PCI bus; See col. 6, lines 43-47), wherein
    - the bridge (i.e., said PCI-to-PCI Bridge) also supports a memory read and a memory read line command (See col. 10, lines 30-64); and
    - the bridge (i.e., said PCI-to-PCI Bridge) prefetches a programmable size of data (See Fig. 6 and col. 9, lines 20-44; i.e., PCI-to-PCI Bridge prefetches data with a fetch size in F2 field of a prefetch control register for multiple command, and with a fetch size in F1 field of the prefetch control register for memory read line command).

Peters does not teach that the programmable size of data is dynamically decided based on a PCI cycle type.

Hopkins discloses a prefetching variable length data (See Abstract), wherein

- a first bus (i.e., System Bus 10 of Fig. 1);
- a second bus (i.e., PCI I/O Bus 20 of Fig. 1); and
- a bridge (i.e., Interface Unit 30 of Fig. 1) coupling the first bus to the second bus (See col. 3, lines 39-41), wherein
    - the bridge (i.e., said Interface Unit) is configured to allow a PCI Master accessing the first bus to dynamically decide a prefetch size of data based on a PCI cycle type (See col. 5, line 64 through col. 6, line 20 and col. 9, lines 42-52, wherein in fact that the prefetch size could vary dynamically depending upon the device that is making the read request on PCI bus impliedly suggests that the bridge is configured to allow a PCI Master (i.e., PCI device 40 in Fig. 1) accessing the first bus (i.e., System Bus 10 of Fig. 1) to dynamically decide a prefetch size of data

based on a PCI cycle type (i.e., upon a read request signal from a specific PCI device)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said prefetching variable length data, as disclosed by Hopkins, in said method of operating said bridge (i.e., operating PCI-to-PCI Bridge), as disclosed by Peters, for the advantage of making said bridge more efficient use of the bandwidth of the slower second bus, as compared to conventional approach (See Hopkins, col. 3, lines 5-22).

Response to Arguments

9. Applicant's arguments filed on 28th of February 2006 with respect to claims 1, 15, and 16 have been considered but are moot in view of the new ground(s) of rejection.

In particular, the Examiner brought Hopkins reference in the rejection for the limitations which are not provided by Peters, AAPA, and Corrigan and all of the other art cited (See *Claim Rejections - 35 USC § 103*).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

PCI Local Bus Specification published by PCI Special Interest Group, Revision 2.2, December 18, 1998.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Patent Examiner
Art Unit 2112

CEL/